AF/GAU - 2754

Patent

Arlene 12/18/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Vora

Art Unit: 2512

Examiner: Sara Crane

Serial No. 08/654,760

Filed: 5/29/96

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

Box AF

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
December 7, 1998

APPELANT'S REPLY BRIEF

Dear Sir:

In response to the Examiner's Answer mailed 11/10/98, please find below the Appellant Reply Brief for the above identified case as follows.

ARGUMENT IN REPLY TO EXAMINER'S ANSWER

This whole appeal really turns around one simple issue. The Examiner has misunderstood the teachings of the Mori reference and not assigned proper meaning to the term "self aligned" in the claims on appeal. Simply put, the appellant's memory cell is much smaller than the prior art because it uses a self aligned floating gate which never ever extends beyond the lateral edges of the well. The applicant's memory cell is manufactured using an anisotropic etch to form the floating gate such that all horizontal components of the floating gate conductive polysilicon are removed leaving only the vertical portions on the sidewalls of the well in which the vertically oriented flash

EEPROM is made. This is clearly shown in the applicant's figures and steps 33 and 34 in the table entitled SELF ALIGNED MEMORY CELL toward the end of the applicant's specification. It should be noted that the memory cell is comprised of a single vertically oriented EEPROM transistor and the term self aligned in the title of this table will be understood by those skilled in the art to mean a self aligned floating gate among other things because that is a big part of what makes the applicant's flash EEPROM memory cell so small which was clearly stated to be the object of the invention.

The principal error made by the Examiner in this case was in misinterpreting the teachings of the Mori reference in assuming from the appearance of the drawings of the Mori cell that the Mori floating gate is self aligned. The undersigned believes this error was made because the drawings (Figures 1a and 1b) of the Mori cell shows the floating gate FG having both a vertical and a horizontal component near the top of the well and a horizontal component in the bottom of the well, but it shows the edge of the horizontal component at the top of the well cut off and aligned with the edges of the well.

What the Examiner has either accidentally overlooked or intentionally ignored is the fact pointed out by the undersigned that the Mori reference at Col. 9, lines 28-9 teaches use of a mask to pattern and etch to define the floating gates. Exhibit A attached is the pertinent portion of the Mori reference which teaches patterning and etching to form the floating gate. Patterning, as is well known to those skilled in the art, means using a mask to pattern photoresist to be used as an etch mask to define the structure of a layer under the photoresist.

The fundamental error which the Examiner has made here is that she assumes that in a micron sized structure, when a mask is used to define the edges of the floating gate, the positions of those edges can be

guaranteed ev ry time to b aligned with th edges of the trench. As is well known in the semiconductor processing art, this is simply not true because registration errors of the mask in aligning it with the positions of the trenches will cause uncertainty in the position of the edges of the floating gate formed using the mask. Exhibit B attached in an article in the prior art on optical photolithography written by a scientist at Bell labs. This article at page 471 shows that several research groups have implemented 1 micron photolithography to pattern photoresist to fabricate memory cells and typically experienced plus or minus 0.3 micron level-to-level registration errors. This means that it is well known in the art that when a mask is used to fabricate a structure on one layer, there is uncertainty where that structure will be registered relative to the underlying layer and the misregistration is typically plus or minus 0.3 microns. This further means that because Mori used a mask to pattern and etch the floating gate, the edge of the floating gate so formed may be up to plus or minus 0.3 microns away from the edge of the trench and where it will be within this production tolerance exactly is not predictable from one batch of chips to the next. This further means that structure overlying the floating gate which must be registered to it for proper positioning to make the device work must be spaced far enough away from it to make sure that the uncertainty of its exact boundary are accounted for so that an overlap that would render the device inoperative does not occur.

With the self aligned process of the claimed invention, there are no registration errors to worry about as it is guaranteed everytime that the floating gate will be completely contained within the perimeter of the well. Therefore structures that are formed that need to be registered to the floating gate can be closer because there is no uncertainty as to the exact location of the floating gate boundary. This means that the

applicant's cell can be made much smaller, and this is what the Vora Declaration is all about (Vora is the applicant and appellant). The Vora declaration compares the sizes of the Mori cell and the size of his cell and points out why his cell can be smaller using the same design rules because of the certainty of the position of the Vora cell floating gate and the uncertainty of the position of the Mori cell floating gate.

It is clear, contrary to the Examiner's argument, that the applicant has presented evidence that the process limitation "self aligned" gives rise to structural differences over the prior art. That evidence is the portion of the Mori specification that teaches use of a mask to form the floating gate. This means to persons skilled in the art that there is no way to predict exactly where the edge of the floating gate will be relative to the edge of the well. In this sense, the drawings of the Mori cell in his patent are highly deceptive in that they show a floating gate aligned with the edges of the well despite the fact that there is no guarantee that that is exactly where they will actually be every time. Since the Vora cell floating gate is guaranteed to be fully contained within the well perimeter because the anisotropic etch takes off all floating gate poly that is horizontal up above the top of the well on the top of the substrate. This is a significant structural difference that defines the essence of the structural difference over the prior art which gives it the advantages pointed out by the Vora declaration.

The Vora cell also uses a bit line which is not buried in the substrate, and this too contributes to the ability to make the Vora cell smaller for the reasons detailed in the appeal brief.

Contrary to the Examiner's argument, the applicant is not asking the Board to take judicial notice that the claim language means something other than what it says or trying to get the Board to read limitations from the specification into the claim. The

applicant is simply asking the Board to properly interpret the claims in light of the teachings of the applicant's specification. The Federal Circuit has noted this distinction in Phonometrics, Inc. v. Northern Telecom Inc., 45 USPQ2d 1421 (Fed. Cir. 1998). There the Federal Circuit was interpreting the meaning of a "call cost register means" in accordance with the teachings in the specification that it both provided a display of the total cost at the end of the call as well as continuously reminding the caller of the cost of the call as the call progressed. Phonometrics argued that the Federal Circuit was reading limitations into the claim from the specification. The Federal Circuit held that this was not what was happening and all they were doing was interpreting a limitation that was specifically recited in the claim in light of the teachings of the specification. Specifically, the Federal Circuit held at p. 1427:

> Phonometrics of course argues that additional limitations cannot be imported into a claim from a written description. We mayu, however, construe a specifically claimed limitation in light of the specification, which is all we do here.

The Examiner argues that the applicant's specification does not teach a process for making a self aligned floating gate despite the fact that the applicant's specification clearly includes a table at page 13 which summarizes a process to make a self aligned cell including steps 33 and 34 which define the anisotropic etch that forms the self aligned floating gate by etching away all horizontal components of the layer of polysilicon from which the floating gate is formed. These two steps in conjunction with the detailed description earlier in the specification and the figures clearly shown how a floating gate is formed which is self aligned so as to not extend beyond the edges of the trench by using an anisotropic etch instead of the mask of the Mori prior art.

As to the bit lines formed on the surface of the substrate, the applicant requests that the Board take notice that in the Mori cell embodiment with a bit line on the surface, there must be a contact hole formed at every cell. This contact hole must be defiend with a mask meaning that alignment tolerances around the contact hole must be used. This means all the structures around the contact hole that must not overlap with it must be spaced further away from it. This makes the Mori cell larger than the Vora cell which does not require a contact hole formed using a mask at each cell.

The applicant notes that the Examiner has actually properly interpreted the "self aligned" claim limitation at page 10 of her answer in the sense that she notes that it will not extend beyond the edges of the trench. This is partially correct. The correct interpretation is that it will not have any horizontal component on the surface of the substrate or on the bottom of the well and therefore will not extend beyond the perimeter of the trench. However, even with the Examiner's interpretation, the Vora cell distinguishes over the Mori prior art because the Mori prior art defines a floating gate which will extend beyond the perimeter of the trench because it is made with a mask and registration errors guarantee uncertainty in the location of the edges of the Mori floating gate relative to the edges of the trench.

As a final note, Exhibit C attached is a copy of the cover letter sent with the hand carried copy of the formal response to the final rejection in the form of an amendment and Vora Declaration which was hand carried to Examiner Crane when the undersigned learned that the mailed version of the formal response had not yet reached the Examiner. This cover letter was stamped by the Group Receptionist with a date of receipt of July 20, 1998.

All claims are believed to be in condition for allowance, and favorable action is

ernestly solicited.

Respectfully submitted,

Dated: December 7, 1998

Ronald Craig Fish
Reg. No. 28,843
Tel 408 778 3624
FAX 408 776 0426

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on 12/8/98
(Date of Deposit)

Ronald Craig Fish, President
Ronald Craig Fish, a Law Corporation
Reg. No. 28,843

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trench, and indeed, that width is slightly greater than the width of the drain bitline (see, Fig. 1*b*).

This configuration provides continuous source regions and drain regions around each trench. As a result, the channel region is also continuous around each trench, thereby maximizing the channel interface to the floating gate, and optimizing charging efficiency.

2.3. Gate Conductor Formation. The third stage of fabrication involves forming the vertical floating gate and program gate conductors, and associated insulating layers.

Referring to FIG. 4*b*, after trench formation, an gate oxide layer 74 is grown over the sidewalls and bottom of each trench 72, to a thickness of about 200 Angstroms. During this procedure, some small amount of oxide will also be grown onto the thick oxide.

Next, a first polysilicon layer 80, which will form the floating gates for the memory cells, is deposited over the oxide layer 71, and into each trench. This poly 1 layer is deposited to a thickness of about 3000–5000 Angstroms, and highly doped N+with phosphorous to render it conductive.

The poly 1 deposition forms a conductive layer within each trench, including a vertically extending section 82. The vertically extending section 82 overs the gate oxide 74 on the sidewalls of the trench, leaving a central cavity 84 in the trench.

The poly 1 layer is then patterned and etched to define the floating gates.

Referring to FIGS. 1, 1*a* and 1*b* after definition of the vertical floating gates FG, the text step is to grow over the substrate an interlevel oxide layer ILO. This interlevel oxide layer grows over the poly of the floating gates to a thickness of about 300 Angstroms. Alternatively, an oxide/nitride/oxide layer of equivalent oxide (electrical) thickness may be used.

Next, a second polysilicon layer which will form the program gates PG for the memory cells, is deposited over the substrate and into each trench cavity (84 in FIG. 4*b*). The poly 2 fills the trench cavity, and is insulated from the floating gate conductors FG by the interlevel oxide ILO. This poly 2 layer is deposited to a thickness of about 3000–5000 Angstroms, and highly doped N+with phosphorous to render it conductive.

The poly 2 deposition forms a vertically extending conductive program gate element PG within each trench. The vertically extending program gate overlaps the vertically extending portion of the floating gate, providing capacitive coupling between the program gate and the insulated floating gate.

The poly 2 layer 20 is then patterned and etched to define the wordlines WL (see, FIG. 1*b*), which incorporate the program gates PG.

3. Conclusion. Although the invention has been described with respect to exemplary embodiments, various changes and modifications of the disclosed embodiments, as well as alternative embodiments, will be suggested to one skilled in the art. It is, therefore, intended that the invention encompass such changes and modifications as fall within the scope of the appended claims.

What is claimed is:

1. A method of fabricating a vertical memory cell array, using vertical floating gate FET memory cells, in a substrate of a first conductivity type, comprising the steps:

forming in the substrate multiple rows of doped groundline zones of a second conductivity type extending down to a selected groundline depth;

into each groundline zone, forming a doped channel zone of the first conductivity type extending down to a selected source/channel junction depth, thereby defining a buried source groundline between the source/channel junction and the groundline depth;

into each channel zone, forming a doped drain bitline of the second conductivity type extending down to a selected drain/channel junction depth, thereby defining a buried channel layer between the drain/-channel junction and the source/channel junction;

in each bitline row, forming multiple trench areas through said drain bitline, said channel layer and at least partially into said source groundline, thereby defining drain, source and channel regions adjacent each trench, each trench further having substantially vertical sidewalls;

for each trench, forming a gate insulator layer over the substantially vertical sidewalls of said trench;

for each trench, forming a floating gate conductor disposed into the trench, insulated from the associated channel region by the gate insulator;

forming an interlevel insulator layer over said floating gate conductor; and

forming onto the substrate multiple columns of program gate worline conductors extending over respective columns of trenches, insulated from said floating gates by said interlevel insulator.

2. The method of fabricating a vertical memory cell array of claim 1, wherein, for each trench, said floating gate is formed over the sidewalls of such trench defining, a central cavity, and the program gate conductor is disposed into such cavity.

3. The method of fabricating a vertical memory cell array of claim 2, wherein the trench is substantially square in horizontal cross section and has substantially vertical sidewalls.

4. The method of fabricating a vertical memory cell array of claim 1, wherein the trench is surrounded by the source groundline and drain bitline.

5. The method of fabricating a vertical memory cell array of claim 1, wherein said source groundline and drain bitline are doped N+.

6. The method of fabricating a vertical memory cell array of claim 1, wherein the memory array is an EPROM.

7. The method of fabricating a vertical memory cell array of claim 1, wherein said drain bitline, channel zone and groundline zone are formed by respective implant/diffusion procedures.

8. A method of fabricating a vertical memory cell array, using vertical floating gate FET memory cells, in a substrate of a first conductivity type, comprising the steps:

forming in the substrate multiple rows of doped groundline zones of a second conductivity type extending down to a selected groundline depth;

into each groundline zone, forming a doped channel zone of the first conductivity type extending down to a selected source/channel junction depth, thereby defining a buried source groundline between the source/channel junction and the groundline depth;

into each channel zone, forming a doped drain bitline of the second conductivity type extending down to a selected drain/channel junction depth, thereby defining a buried channel layer between the drain/-channel junction and the source/channel junction;

EXH. A

Patent

Took Docs to Examiner Crane. Crane would not sign and sent me to group receptionist to have Docs stamped in.

TES PATENT AND TRADEMARK OFFICE

Art Unit: 2811

Examiner: Sara Crane

H EEPROM FOR GREATER DENSITY AND LOWER COST

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
July 14, 1998

Attn: Examiner Crane, Building CP4, Floor 06 Room B06

Dear Sir:

In response to a telephone conversation with Examiner Crane regarding the subject case indicating that she has not as yet received the formal response we mailed on June 9, 1998, enclosed is a hand delivered copy of the amendment we filed on June 9, 1998, a Declaration of Madhu Vora dated June 9, 1998, a copy of the postcard return receipt indicating that these two documents were received on June 12, 1998 by the PTO, a copy of a supplemental response mailed June 10, 1998 enclosing two drawing markups that were inadvertantly omitted from the June 9, 1998 amendment and a postcard return receipt indicating that the supplemental amendment was received at the PTO on June 15, 1998. I would appreciate a review of the new evidence and the response and a telephone call at 408 778 3624 regarding status of the case after you have reviewed the new evidence. Our position is that the claims were misinterpreted by

Exh C

Examiner Giordina and she misunderstood the prior art disclosure either reason alone being suffiicient to invalidate the prima facie case of obviousness leaving the claims rejected on invalid grounds.

All claims are believed to be in condition for allowance, and favorable action is ernestly solicited.

Respectfully submitted,

Dated: July 14, 1998

Ronald Craig Fish
Reg. No. 28,843
Tel 408 778 3624
FAX 408 776 0426

I, Sara Crane, certify that the documents described above were hand delivered to me on _____ in building CP4, Floor 6, Room B06 along with a copy of a return receipt postcard indicating that the Amendment dated 6/9/98 and the Declaration of Madhu Vora dated 6/9/98 were received by the PTO mail room on June 12, 1998 and a copy of a return receipt postcard indicating the Supplemental Response dated 6/10/98 and its enclosed drawing markups was received by the PTO mail room on 6/15/98.

_____ _____
Sara Crane Date

12 Lithography

R. K. WATTS
AT&T Bell Laboratories
Murray Hill, New Jersey

12.1 INTRODUCTION

A larger fraction of the cost of a modern production facility for integrated circuits is spent for lithographic systems than for any other type of process equipment. The lithographic equipment is the most complex—and therefore should be considered the most likely to fail—of the many components of the production line. In these aspects, it is the most important part of the line.

This chapter examines the status of each of a variety of high-resolution lithographic techniques in the late 1980s. Representative commercially available systems are mentioned along with systems under development. Projections are made for each technique to show what, if anything, can be done to allow it to meet the future needs of the industry. Resolution is emphasized because it lends itself to analysis more readily than any other facet of the subject. For example, advances in the precision of level-to-level registration depend on progress in optical and mechanical engineering practice; there is no theoretical underpinning.

12.2 OPTICAL LITHOGRAPHY

Projection printing is the imaging of a mask pattern onto a wafer by means of an optical projection system. Because it combines high resolution with low defect density, it is the favored optical method. For a given number of resolution points or smallest features resolvable by the system (typically 10^8–10^9), smaller features are obtained in the image if the image field is kept small.

Available systems are of three types. In the reduction wafer stepper[1] an image of a mask reticle, reduced typically five or ten times, is exposed on the wafer, then stepped to a neighboring position and exposed again, and so on until the whole wafer is patterned. The large reticle pattern is easy to produce and to inspect for defects. Refractive optics are employed. In the 1:1 Ultratech stepper, the reticle pattern is the same size as the image pattern, and the optics are refractive and reflective.[2] In the Perkin Elmer printer, mask and image patterns are also the same size, but mask and wafer are scan through highly corrected portions of the ob merical aperture of this last system makes

12.2.1 A Benchmark: 1 μm Photolitho;

Before considering submicron lithography reference, the requirements and the practic with design rules of 1 μm. Such a design linewidth and the minimum spacing betwe window is 1 × 1 μm, and the maximum a ±0.25 μm. Let us see how several groups into practice.

In 1980, Sigusch et al.[4] of Siemens use duction lens of numerical aperture (NA) toresist 1.5 μm thick. Test circuits, incl linewidths of 1 μm were fabricated. Line metal and field oxide levels and within window levels. Registration errors were l Siemens[5] reported extending this process resolution Zeiss lens of NA 0.42, again radiation. In this case, linewidth variatio metal level and within ±0.1 μm for the quoted, but the maximum error allowed b

Hillis et al.[6] of Hewlett-Packard have cess for the production of chips for the H contain as many as 6.6×10^5 transisto photoresist, it was not possible to keep ±0.1 μm and the authors w re forced to fications. This bilayer resist system, sh lower layer of poly methyl methacrylate planar surface than the underlying circui thinner layer of Kodak 809 positive phc 436 nm radiation of the stepper, to wh added to the PMMA to minimize reflect opment, the top layer serves as a co PMMA with shorter wavelength radiati

In 1983, Orlowsky et al.[7] of AT&T process. A wafer stepper with a Tropel expose a trilayer resist structure, shown ter resist exposure, a thin layer of SiC patterned by reactive ion etching (RIE) reactive ion etching of the underlying HPR206 photoresist. Linewidth errors than ±0.1 μm. Level-to-level registra

EXH. B

same size, but mask and wafer are scanned continuously and synchronously through highly corrected portions of the object and image fields.[3] The smaller numerical aperture of this last system makes it unsuitable for submicron imaging.

12.2.1 A Benchmark: 1 μm Photolithography

Before considering submicron lithography, we shall first examine, as a point of reference, the requirements and the practice of photolithography for MOS circuits with design rules of 1 μm. Such a design rule generally means that the minimum linewidth and the minimum spacing between lines is 1 μm; the minimum contact window is 1 × 1 μm, and the maximum allowed misregistration between levels is ±0.25 μm. Let us see how several groups of workers have put 1 μm lithography into practice.

In 1980, Sigusch et al.[4] of Siemens used a wafer stepper with a Zeiss 10× reduction lens of numerical aperture (NA) 0.28 to expose AZ1450J positive photoresist 1.5 μm thick. Test circuits, including a 16 kbit SRAM, with minimum linewidths of 1 μm were fabricated. Linewidth errors were within ±0.1 μm for metal and field oxide levels and within ±0.2 μm for polysilicon and contact window levels. Registration errors were less than ±0.5 μm. In 1982, workers at Siemens[5] reported extending this process to 0.75 μm design rules using a higher resolution Zeiss lens of NA 0.42, again exposing 1.5 μm of resist with 436 nm radiation. In this case, linewidth variations were kept within ±0.15 μm for the metal level and within ±0.1 μm for the other levels. Registration errors are not quoted, but the maximum error allowed by the design rule is ±0.3 μm.

Hillis et al.[6] of Hewlett-Packard have reported implementation of a 1 μm process for the production of chips for the HP9000 computer. Some chips of the set contain as many as 6.6×10^5 transistors. With a wafer stepper and standard photoresist, it was not possible to keep linewidth variations within the required ±0.1 μm and the authors were forced to employ a bilayer resist to meet the specifications. This bilayer resist system, shown in Fig. 12.1*b*, incorporates a thick lower layer of poly methyl methacrylate (PMMA), which provides a more nearly planar surface than the underlying circuit topography on which to apply the upper thinner layer of Kodak 809 positive photoresist. The top layer is exposed by the 436 nm radiation of the stepper, to which the PMMA is insensitive. A dye was added to the PMMA to minimize reflections of the 436 nm radiation. After development, the top layer serves as a conformal mask for flood exposure of the PMMA with shorter wavelength radiation.

In 1983, Orlowsky et al.[7] of AT&T Bell Laboratories reported a 1 μm NMOS process. A wafer stepper with a Tropel 5× reduction lens of NA 0.35 was used to expose a trilayer resist structure, shown in Fig. 12.1*c*, with 405 nm radiation. After resist exposure, a thin layer of SiO_2 (plasma-deposited) beneath the resist is patterned by reactive ion etching (RIE). The SiO_2 then serves as a stencil mask for reactive ion etching of the underlying thick polymer layer, usually hard-baked HPR206 photoresist. Linewidth errors for the important polysilicon level were less than ±0.1 μm. Level-to-level registration errors were typically ±0.3 μm or less.

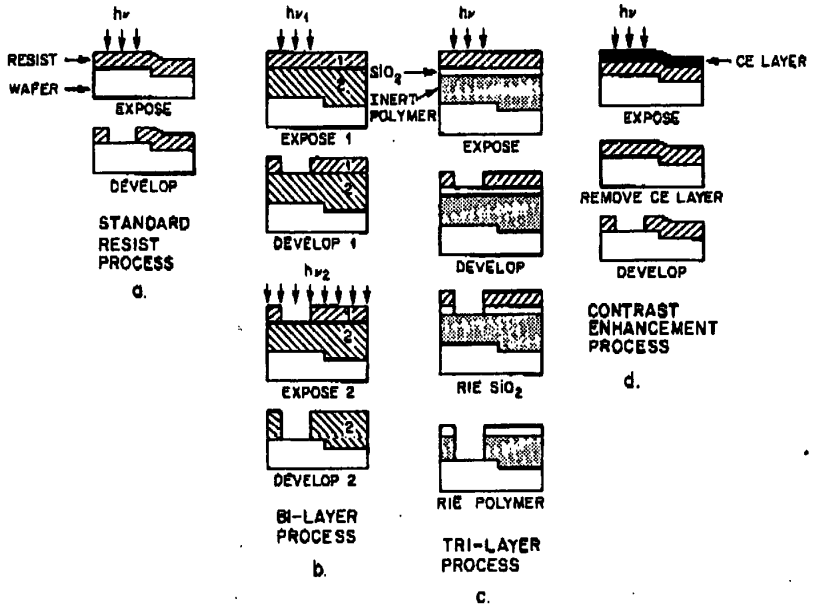

Fig. 12.1 Resist processes: (*a*) single-layer resist, (*b*) bilayer resist, (*c*) trilayer structure, (*d*) contrast enhancement process.

The trilayer process is not well suited to high-volume production because of the slow and rather involved processing.

A fourth popular resist process is shown in Fig. 12.1*d*. In this scheme, called contrast enhancement (CE), a thin layer of bleachable material is spun over the positive photoresist.[8] Upon exposure, the illuminated areas of the bleachable CE layer become more transparent as exposure progresses. Ideally, a part of the pattern that should receive no exposure, corresponding to an opaque feature on the mask, would receive none. But, of course, some light from nearby features corresponding to transparent parts of the mask spills over to these regions. The transmission of the CE layer is greater the higher the intensity of the light incident on it. Thus, the contrast, or ratio of maximum light intensity to minimum intensity in the pattern, of the radiation exposing the underlying resist is increased or enhanced. This process increases resolution and linewidth control.

The following conclusions can be drawn from these reports. Wafer steppers available in 1980–1983 provided adequate resolution for 1 μm lithography. Some workers found it necessary to employ a more complex multilayer resist scheme to obtain adequate linewidth control.

The level-to-level registration provided by the full wafer alignment scheme, wherein the reticle is first aligned to the wafer and then each field is exposed in turn, was barely adequate. A more accurate method in which each exposure field is separately aligned is now common practice. The registration errors are not due to pattern placement errors on the reticle. F a reticle, formed by plotting the placement 100 × 100 mm array. The maximum error error in the 5× or 10× reduced image of the requirements of 1 μm lithography.

12.2.2 Limits of Photolithography

Figure 12.3 shows a general schematic rep object plane is the mask or reticle. It is illu shown) and imaged by the projection optic the wafer. We consider in turn two extrem of the mask and spatially incoherent illum limit. This situation has been treated by Bo quote some of their results.

If the mask is illuminated by a point sou tion between the field amplitudes $U_0(x_0, y_0)$ (The phase at each point x_0, y_0 on the object k is the propagation constant of the wave and

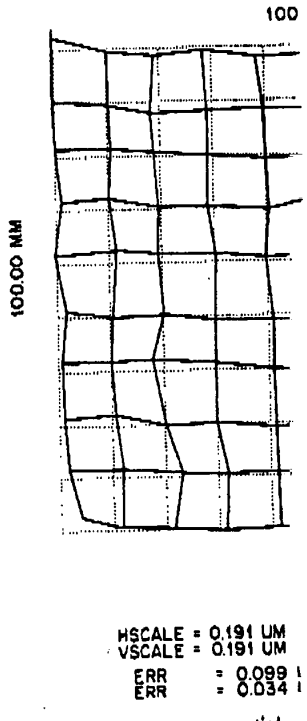

Fig. 12.2 Map f placement errors on a reticle.

to pattern placement errors on the reticle. Figure 12.2 shows a typical error map of a reticle, formed by plotting the placement errors measured at 100 locations in a 100 × 100 mm array. The maximum error is only 0.099 μm. The corresponding error in the 5× or 10× reduced image of the reticle is negligible compared with the requirements of 1 μm lithography.

12.2.2 Limits of Photolithography

Figure 12.3 shows a general schematic representation of an imaging system. The object plane is the mask or reticle. It is illuminated by an illumination system (not shown) and imaged by the projection optics onto the image plane, which will be the wafer. We consider in turn two extreme cases: spatially coherent illumination of the mask and spatially incoherent illumination of the mask in the diffraction limit. This situation has been treated by Born and Wolf,[9] among others; we shall quote some of their results.

If the mask is illuminated by a point source, then there is a definite phase relation between the field amplitudes $U_0(x_0, y_0)$ at different points on the object plane. (The phase at each point x_0, y_0 on the object plane is simply given by $\mathbf{k} \cdot \mathbf{r}$, where $\mathbf{k}$ is the propagation constant of the wave and $\mathbf{r}$ is the path from the source to x_0, y_0.)

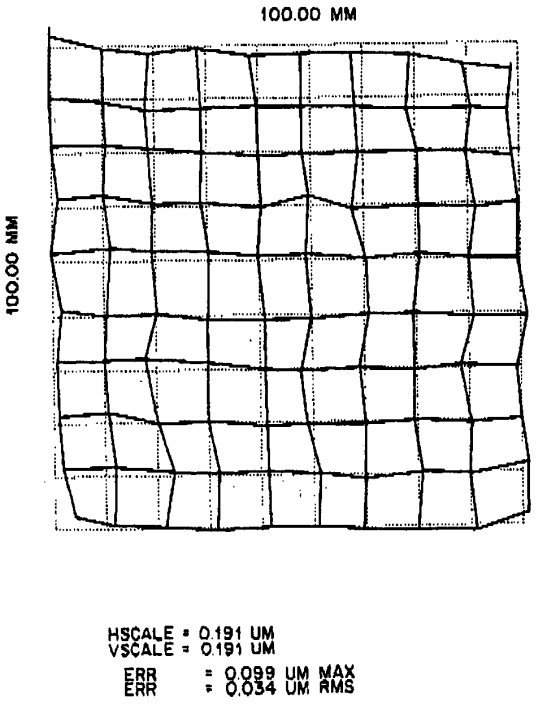

Fig. 12.2 Map of placement errors on a reticle. The dotted grid represents c rrect placement.

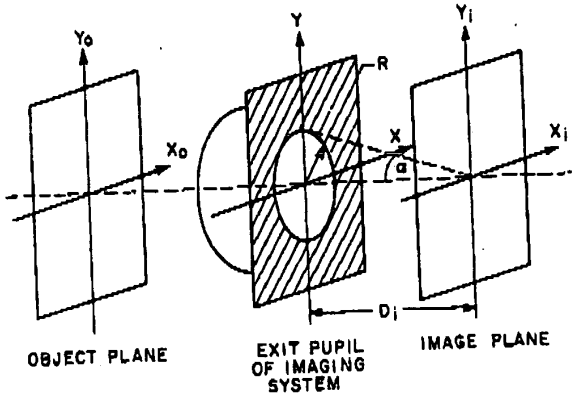

Fig. 12.3 Schematic representation of an imaging system. R is the radius of the exit pupil.

The illumination is said to be spatially coherent. Then the Fourier transform $G_0(u, v)$ of $U_0(x, y)$ is related to $G_i(u, v)$, the Fourier transform of the amplitude $U_i(x_i, y_i)$ in the image plane, by the relation

$$G_i(u, v) = H(u, v)G_0(u, v), \tag{1}$$

where $H(u, v)$ is the coherent transfer function. $H(u, v)$ is the (spatial) frequency response of the optical system. For a round pupil of radius R (see Fig. 12.3), $H(u, v)$ is given by

$$\begin{aligned} H(u, v) &= 1 \quad \text{if } \sqrt{u^2 + v^2} \le \frac{R}{\lambda D_i} \\ &= 0 \quad \text{if } \sqrt{u^2 + v^2} > \frac{R}{\lambda D_i}. \end{aligned} \tag{2}$$

λ is the wavelength of the illuminating light. H is plotted in Fig. 12.4, where the spatial frequency u is normalized by dividing it by the spatial frequency u_M, where

$$\begin{aligned} u_M &= \frac{2R}{\lambda D_i} = \frac{1}{\lambda F} \\ &= 2\left[\frac{1}{\lambda\sqrt{(NA)^{-2} - 1}}\right]. \end{aligned} \tag{3}$$

where F is the f number of the projection system, $F \equiv D_i/2R$, and NA is the numerical aperture, $NA = \sin\alpha = R/\sqrt{D_i^2 + R^2}$. The spatial frequency u is usually measured in line pairs, or cycles, per mm. The inverse of u is a feature size. In this case, the feature is a grating of equal lines and spaces; u^{-1} is the period of the grating.

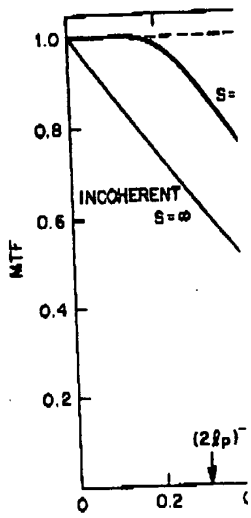

Fig. 12.4 Modulation transfer functions imaging plotted vs. normalized spatial fre

In the opposite extreme, where the fore no definite phase relation betwee illumination is said to be incoherent. I Eq. (1) between the Fourier transfor *intensities*, the squares of the wave a

$$G_i(u, v) -$$

where H is called the optical trans modulation transfer function (MTF). expression analogous to equation (2)

$$H(u) = \frac{2}{\pi}\left[\cos^{-1}\left(\right.\right.$$

for $u \le u_M$. The limiting frequency coherent illumination ($u/u_M = 0.5$).

The transfer function describes h image of a sinusoidal grating object lation in a grating of spatial frequen

$$M(u)$$

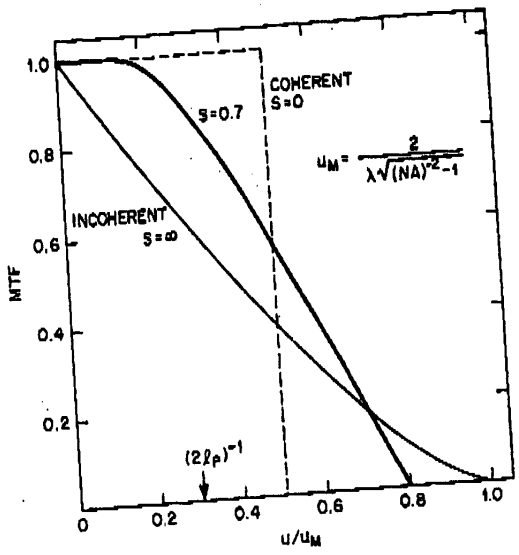

Fig. 12.4 Modulation transfer functions for coherent, partially coherent, and incoherent imaging plotted vs. normalized spatial frequency.

In the opposite extreme, where the light source is very large and there is therefore no definite phase relation between two points on the object plane (mask), the illumination is said to be incoherent. In this case, there is a relation such as that of Eq. (1) between the Fourier transforms G_0 and G_i of the object and image plane *intensities*, the squares of the wave amplitudes, given by

$$G_i(u,v) = H(u,v)G_0(u,v)\,, \tag{4}$$

where H is called the optical transfer function. The absolute value $|H|$ is the modulation transfer function (MTF). It is also plotted in Fig. 12.4. The analytical expression analogous to equation (2) can be written for H. It is

$$H(u) = \frac{2}{\pi}\left[\cos^{-1}\left(\frac{u}{u_M}\right) - \frac{u}{u_M}\sqrt{1-\left(\frac{u}{u_M}\right)^2}\right], \tag{5}$$

for $u \le u_M$. The limiting frequency is twice as great ($u/u_M = 1$) as in the case of coherent illumination ($u/u_M = 0.5$).

The transfer function describes how the optical projection system degrades the image of a sinusoidal grating object pattern of equal lines and spaces. The modulation in a grating of spatial frequency u is $M(u)$, where

$$M(u) = \frac{I_M(u) - I_m(u)}{I_M(u) + I_m(u)}. \tag{6}$$

I_M and I_m are the maximum and minimum intensities, respectively, in the grating pattern. The MTF at frequency u is the ratio of image modulation to object modulation,

$$MTF = \frac{M_i(u)}{M_0(u)}. \tag{7}$$

Although the sine wave formulation is more convenient mathematically, the MTF is always measured experimentally for an equal line/space or clear/opaque grating pattern (of periodicity u^{-1}) on a mask. That is, the object is a square wave, not a sine wave. For the incoherent case, there is a simple relation between the sine wave and the square wave MTFs.[10]

In modern printers, the illumination is intermediate between the coherent and incoherent limits. The separation between points in the object that have correlated phases is neither infinite nor near zero. It can sometimes be varied by means of a diaphragm in the condenser illuminating the mask. This is a familiar phenomenon to anyone who has used a microscope. As the aperture stop diaphragm is closed, the image looks "sharper," but interference rings finally appear around edges, and the light level drops. This is the near-coherent case. Opening the diaphragm causes the rings to disappear and the image becomes brighter. The ratio S of the numerical aperture of the condenser to that of the projection optics is often used as a measure of coherence. $S = 0$ implies near-coherence; if $S = 1$, the apertures are matched and the entrance pupil of the projection optics is filled to give near incoherent illumination. Further increase of S just causes more light scattering. $S = \infty$ corresponds to the incoherent limit. Partial coherence ($0 < S < 1$) has some advantages over incoherent illumination. The useful range,[11] MTF > 0.6, is extended to higher spatial frequencies. Edge gradients in the image become steeper, and the image is a little less sensitive to defocus. Also plotted in Fig. 12.4, is the MTF corresponding to the partial coherence $S = 0.7$. For most projection printers, S has a value between 0.4 and 0.8.

Although most printers have nearly diffraction-limited optics, the aberrations are never zero.[12] Aberrations reduce the MTF. A very important aberration is the focus error. This error might be caused by improper operation of the automatic focus tracking or by departure of the wafer surface from the proper plane. The Rayleigh unit of defocus,

$$w_R = \frac{\lambda}{2(NA)^2}, \tag{8}$$

corresponds to a phase error of $\pi/2$ at the edge of the pupil and is supposed to be the largest focus error which is "imperceptible" to the eye.

Since the transfer functions with round pupil are symmetrical under rotation about the vertical axis, they can be written and displayed as functions of a single variable u, as in Eqs. (5)–(7). However, it is understood that u stands for $\sqrt{u^2 + v^2}$. This two-dimensional nature explains why a small contact window with predominant spatial frequency components $u = v = u_0$ requires a different exposure from

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Wafer steppers are used unde
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possible resolution for a critical
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$S = 0.7$ of Fig. 12.4, this is u_c

$$\ell_{0.6} = 0.$$

In the literature, one often find

where $K = 0.8$ for production
for better conditions.[13]

Table 12.1 gives specificatio
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value of $\ell_P = 0.8\lambda/NA$, the
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layer resist, ℓ_{IL}. (The imagi
to 0.7 μm in thickness.)

There is another reason
MTF curves shown are for

a long line of the same width with $u = u_0$, $v \approx 0$, for $|H(\sqrt{2}\,u_0)|$ is less than $|H(u_0)|$. If both types of features occur on the same mask, both types of resist image will not have correct dimensions. In general, for very small features representing high spatial frequencies, the required exposure depends on the shape of the feature and proximity to other features, setting a practical resolution limit much less than u_M. This is called a "proximity effect."

Wafer steppers are used under many different conditions, ranging from tests by the vendors to operation by scientists and engineers intent on obtaining the highest possible resolution for a critical experiment in device fabrication to operation by less highly skilled personnel in high-volume chip production. As a rough measure of the best resolution obtainable, we take the linewidth $\ell_{0.6} \approx 0.5\, u_{0.6}^{-1}$, where $u_{0.6}$ is the value of u at which the MTF curve of the stepper lens is 0.6. For the curve $S = 0.7$ of Fig. 12.4, this is $u_{0.6}/u_M = 0.48$ giving

$$\ell_{0.6} = 0.52\lambda\sqrt{(NA)^{-2} - 1} \approx \frac{\lambda}{2NA}. \tag{9}$$

In the literature, one often finds the expression for best resolution written as

$$\ell = \frac{K\lambda}{NA}, \tag{10}$$

where $K = 0.8$ for production conditions, and K is some smaller value near 0.5 for better conditions.[13]

Table 12.1 gives specifications of some lenses and the resolutions and depths of focus obtained with them and reported in 1986.[14-18] The field diameter ranges from 7 mm for the lens with largest aperture ($NA = 0.6$) to 20 mm. A larger diameter of the exposure field implies higher throughput, since fewer exposures are necessary. (Throughput, or number of wafers patterned per hour, depends also on wafer size, exposure time, and alignment or registration time. It typically ranges from 10 to 50 wafers per hour for wafer diameter 125 mm or 150 mm.) ℓ_{1L} denotes the resolution obtained over the entire field reported in single-layer positive photoresist of thickness slightly greater than 1 μm, and w_{1L} is the depth of focus measured under these conditions. ℓ_{3L} and w_{3L} are the corresponding quantities measured with trilayer resist. For the second entry in the table, the authors observed the same values for tri-layer resist and for the contrast-enhancement method of Fig. 12.1*d*. As a measure of the quality of the optics, lines 9 and 12 of Table 12.1 give the number of resolution points in the exposure field. Thus, Equation (9) gives a fairly good description of ultimate resolution obtainable in trilayer resist. Also tabulated is the value of $\ell_p = 0.8\lambda/NA$, the best resolution to be expected under production conditions. It is nearly equal to the experimental resolution obtained in thicker single-layer resist, ℓ_{1L}. (The imaging layer in the trilayer structures in Table 12.1 was 0.5 to 0.7 μm in thickness.)

There is another reason for being conservative in estimating resolution. The MTF curves shown are for grating features consisting of equal lines and spaces;

TABLE 12.1 Resolution and Depth of Focus Obtained With Wafer Steppers

Lens	5A3 Nikon	Nikon	10.78.48 Zeiss	Silica Tropel	Silica Matsushita
Reduction	5×	10×	10×	5×	5×
λ(nm)	436	436	365	248	248
NA	0.42	0.6	0.42	0.38	0.35
Field dia. (mm)	20	7	14.1	14.5	14.1
$\ell_{0.6}$ (μm)	0.5	0.4	0.4	0.3	0.4
w_R (μm)	1.2	0.6	1.0	0.9	1.0
ℓ_p (μm)	0.8	0.6	0.7	0.5	0.6
ℓ_{1L} (μm)	0.8	0.6	0.7		0.5
w_{1L} (μm)	2	1			
Resolution points	5×10^8	1×10^8	3×10^8		6×10^8
ℓ_{3L} (μm)	0.6	0.4	0.5	0.5	
w_{3L}	1.5		1	0.5	
Resolution points	9×10^8	2×10^9	6×10^8	7×10^8	
Reference	14	15	16	17	18

they do not apply to other features. A small square feature of size $\ell \times \ell$ is more difficult to resolve than a grating of period 2ℓ, and an isolated line of width ℓ is easier to resolve. For example, with the process reported in Ref. 7, 0.75 μm gates are easily printed and 0.5 μm gates can be printed with somewhat lower yield. However, 0.75 × 0.75 μm contact windows are difficult to print, and 0.5 × 0.5 μm windows are impossible.

The last two columns in the table describe systems that use a KrF excimer laser as light source. Because chromatic aberration of the silica lens is large, the 248 nm radiation must be spectrally narrowed. Figure 12.5 shows 0.5 μm lines produced in trilayer resist with the system of column 4 of Table 12.1. Table 12.2 shows projected specifications of future such systems, kindly provided by V. Pol. Clearly, the last system would need better registration capability if the potentially high resolution is to be useful.

Since resolution of an optical system ~ λ/NA and depth of focus ~ $\lambda/(NA)^2$, it is better to reduce λ than to increase *NA* to improve resolution. A disadvantage

TABLE 12.2 Projected Specifications of Future Deep UV Wafer Steppers[a]

	248/KrF	193/ArF	193/ArF
λ (nm)/laser	0.5	0.38	0.5
NA	15	20	15
Field dia. (mm)	0.3	0.3	0.2
Resolution with trilayer resist (μm)	±0.5	±0.6	±0.4
Focus depth (μm)	±0.1	±0.1	±0.1
Registration, 2σ (μm)			

[a]*Source:* Provided by V. Pol, AT&T Bell Laboratories.

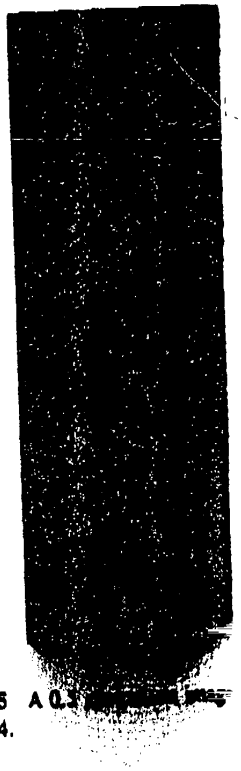

Fig. 12.5 A 0.5 [illegible] lines column 4.

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absorb too strongly; reflective
vacuum for λ < 185 nm. For
Other possible materials for re
they are transparent are CaF_2
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At 248 nm, an MP2400 p
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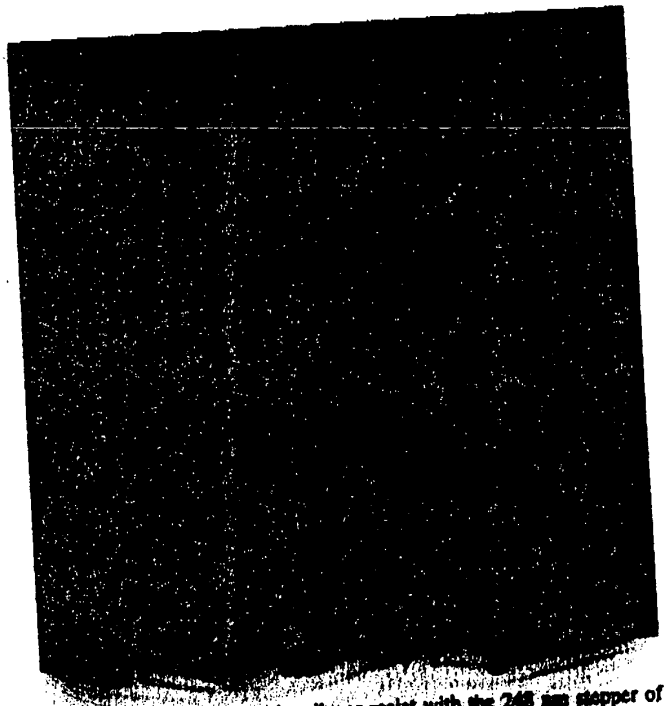

Fig. 12.5 A 0.5 μm pattern imaged in trilayer resist with the 248 nm stepper of Table 1, column 4.

of changing the wavelength is that entirely different resists may be required. Let us see how far this reduction of λ can be carried. For λ < 193 nm, silica lenses absorb too strongly; reflective optics must be used.[19] The optical path must be in vacuum for λ < 185 nm. For λ < 170 nm, the silica reticle absorbs too stongly. Other possible materials for reticle substrates and the spectral regions in which they are transparent are CaF_2 or LaF_3, λ > 130 nm, and MgF_2, λ > 120 nm.[20] These fluoride materials are not now available in the form and quality needed for reticle substrates. Resolution of a system exposing with 130 nm radiation would depend on the value of *NA* that could be achieved and the degree to which aberrations could be corrected—a more difficult task than at longer wavelengths. In addition, the increased Rayleigh scattering ($\sim\lambda^{-4}$) would degrade contrast. It is not likely that systems requiring a stencil reticle for use at even shorter wavelengths will be developed. However, if a mask is used in reflection rather than transmission, then even shorter wavelengths could be used.

At 248 nm, an MP2400 photoresist can be used.[17,21] In the deep ultraviolet spectral region, MP2400 is not as good an image replication medium as it is at slightly longer wavelength. Figure 12.6 shows 0.35 μm lines, which can only be produced in the center of the exposure field, formed in MP2400 by the system of

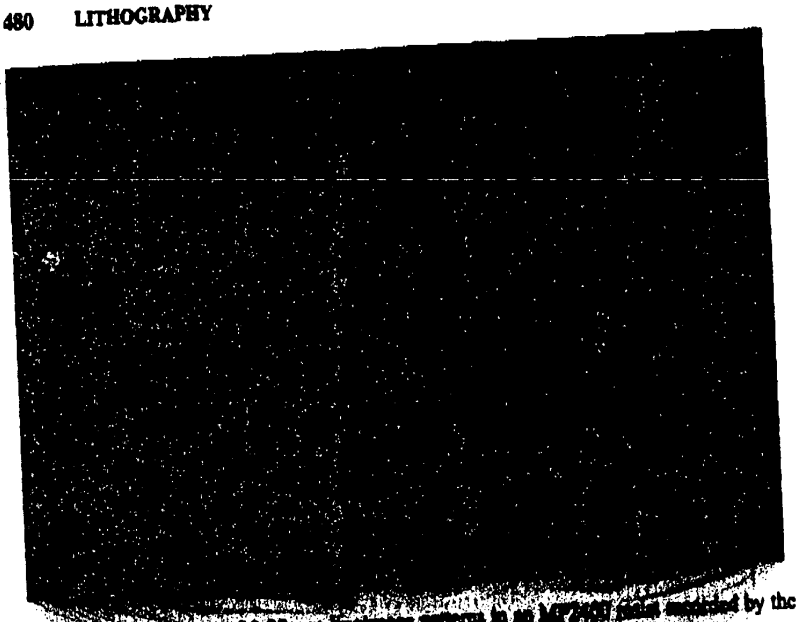

Fig. 12.6 [illegible] of 0.35 μm linespace patterns in an MP2400 resist exposed by the 248 nm stepper of Table 12.1, column 4. The resist is the uppermost layer in a trilayer resist structure.

Table 12.1, column 4. Figs. 12.7*a* and *b* show simulated profiles[21] for this system with an MP2400 resist. The sloped profile of Fig. 12.7*b* matches the experimental profile of Fig. 12.6. The lower part of Fig. 12.7 (*c*, *d*) shows simulated profiles for a fictitious resist with a factor of 3 less absorption at 248 nm than an MP2400. The reduced absorption leads to better profiles. Depth of focus, at least as measured experimentally (the most important measure), depends strongly on resist properties, as can be seen by comparing w_R, w_{IL}, and w_{IL} of Table 12.1.

MP2400 is a two-component positive photoresist. One component is a novolac resin, and the other component is a naphthoquinone diazide dissolution inhibitor. The exposing radiation destroys the inhibition, in this case by an excitation transfer mechanism, and allows the resin to dissolve in the aqueous developer. Because the deep ultraviolet photon has sufficient energy to break bonds, it is also possible to find one-component positive resists that function in the following way. The chain scission produced by the radiation leads to a reduction in molecular weight for some of the molecules. The developer selectively dissolves the part with lower molecular weight. Wolf et al.[22] have studied several resists of this kind. They found that they are less sensitive at 248 nm than an MP2400. Another disadvantage of these resists is their generally poorer resistance to dry etches. An example is poly butene sulfone (PBS). It can be used only with wet etching, as in photomask making.

Most polymeric materials absorb too strongly for $\lambda < 190$ nm.[23] In principle, the new surface sensitization techniques, which do not require deep penetration of

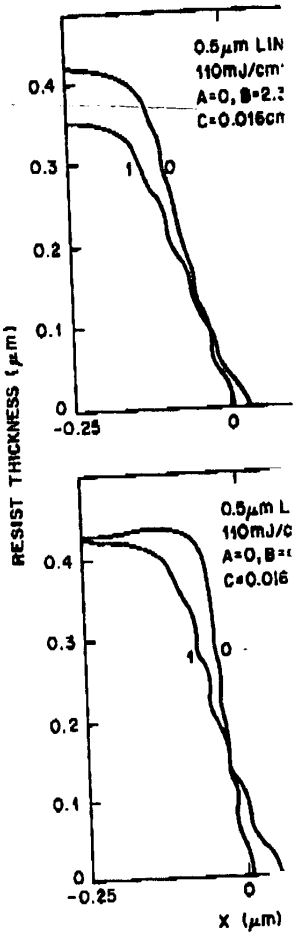

Fig. 12.7 Simulated profil
Table 12.1, column 4, with λ
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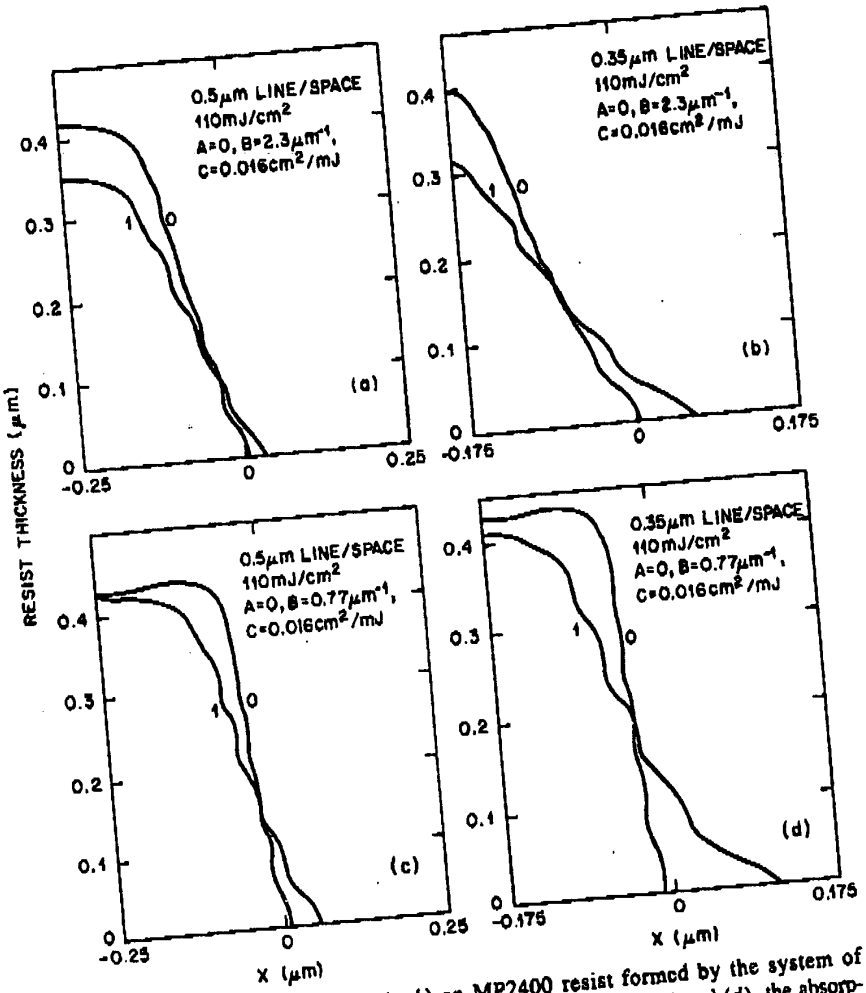

Fig. 12.7 Simulated profiles in (*a*, *b*) an MP2400 resist formed by the system of Table 12.1, column 4, with $\lambda = 248$ nm, $NA = 0.38$, $S = 0.7$. In (*c*) and (*d*), the absorption coefficient of the resist is reduced by a factor of 3. Ref. 21 gives details of the calculation. A, B, and C are model parameters explained in Ref. 20. The photomask covers the portion $x \leq 0$. The 0 and 1 beside the curves indicate perfect focus and defocus by 1 μm, respectively.

the exposing radiation, could be employed.[24,25] A thinner resist, or thinner sensitive top layer, leads to higher resolution (see Table 12.1) and increased depth of focus for lines of given width. Thinner resist also leads to higher defect densities. No concentrated sophisticated effort has been made to reduce defect density in very thin films.

Because of the almost vanishingly small depth of focus accompanying very high resolution, the distance between the imaging system and the wafer must be

seems to be the mask. Ion reduction projection is also attractive. The stencil mask is fragile, but larger than masks for proximity printing. The same issues discussed for X-ray masks in Section 12.4.2 are also of concern of ion-beam masks. Some studies of the effect of the elevated operating temperature of these masks have been reported.[71,78] Dimensional stability may be affected by radiation damage; little is yet known about the stability of these masks.

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Took Docs to Examiner Crane.
Crane would not sign and
Sent me to group receptionist
to have Docs stamped in.

TES PATENT AND TRADEMARK OFFICE

Art Unit: 2811

Examiner: Sara Crane

H EEPROM FOR GREATER DENSITY AND LOWER COST

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
July 14, 1998

Attn: Examiner Crane, Building CP4, Floor 06 Room B06

Dear Sir:

In response to a telephone conversation with Examiner Crane regarding the subject case indicating that she has not as yet received the formal response we mailed on June 9, 1998, enclosed is a hand delivered copy of the amendment we filed on June 9, 1998, a Declaration of Madhu Vora dated June 9, 1998, a copy of the postcard return receipt indicating that these two documents were received on June 12, 1998 by the PTO, a copy of a supplemental response mailed June 10, 1998 enclosing two drawing markups that were inadvertantly omitted from the June 9, 1998 amendment and a postcard return receipt indicating that the supplemental amendment was received at the PTO on June 15, 1998. I would appreciate a review of the new evidence and the response and a telephone call at 408 778 3624 regarding status of the case after you have reviewed the new evidence. Our position is that the claims were misinterpreted by

EXH C

Examiner Giordina and she misunderstood the prior art disclosure either reason alone being suffiicient to invalidate the prima facie case of obviousness leaving the claims rejected on invalid grounds.

All claims are believed to be in condition for allowance, and favorable action is ernestly solicited.

Respectfully submitted,

Dated: July 14, 1998

Ronald Craig Fish
Reg. No. 28,843
Tel 408 778 3624
FAX 408 776 0426

I, Sara Crane, certify that the documents described above were hand delivered to me on _____ in building CP4, Floor 6, Room B06 along with a copy of a return receipt postcard indicating that the Amendment dated 6/9/98 and the Declaration of Madhu Vora dated 6/9/98 were received by the PTO mail room on June 12, 1998 and a copy of a return receipt postcard indicating the Supplemental Response dated 6/10/98 and its enclosed drawing markups was received by the PTO mail room on 6/15/98.

_____ _____
Sara Crane Date